

Original Article

AI-Driven Timing Closure Optimisation for Advanced Semiconductor Designs

VENKATAKRISHNA BRAHMAM POGADADANDA

Senior RTL Design Engineer at AMD-Xilinx, USA.

ABSTRACT: *The complexity of Very Large-Scale Integration (VLSI) and System-on-Chip (SoC) designs has increased tremendously as semiconductor technology has evolved to advanced process nodes such as 7nm, 5nm and beyond. Modern semiconductor designs must meet challenging performance, power and area criteria across multiple voltage domains, manufacturing variations and increasingly complex clocking architectures. Timing closure is one of the most critical and time-consuming challenges in physical design implementation. It has a great impact on the chip performance, manufacturability and time-to-market. Traditional time-optimisation techniques rely heavily on extensive human intervention, iterative engineering procedures, and rule-based tactics that do not scale well with rising design complexity and shrinking process margins. In addition, timing convergence is aggravated by signal integrity, congestion, power limits, process unpredictability and multi-clock synchronisation. This work presents an AI-based timing closure optimisation framework that uses Artificial Intelligence (AI) and Machine Learning (ML) techniques to automate and accelerate timing analysis and optimisation in advanced semiconductor designs. The proposed solution uses predictive analytics, intelligent route classification and adaptive optimisation algorithms to identify major timing violations, provide corrective steps and improve design convergence with minimal human intervention. The system not only accelerates time-constraint detection but also improves decision-making in physical design by learning from prior design information and implementation patterns. A case study on an advanced SoC design demonstrates that the proposed strategy may effectively reduce timing violations, improve slack convergence, shorten engineering turnaround time and increase overall design productivity. The results emphasise that AI-based methods may significantly boost timing-closure efficiency, enabling scalable, reliable, and power-aware semiconductor design for next-generation integrated circuits.*

KEYWORDS: Artificial Intelligence (AI), Timing Closure Optimisation, Semiconductor Design, Electronic Design Automation (EDA), Static Timing Analysis (STA), Machine Learning in VLSI, Advanced Process Nodes, Physical Design Automation, Reinforcement Learning, Predictive Timing Analysis, System-on-chip (SoC), Deep Learning For Chip Design.

1. INTRODUCTION

1.1. BACKGROUND AND INDUSTRY EVOLUTION

The semiconductor sector has undergone a major transformation in the past decade, driven by the growing need for faster, smaller and more energy-efficient electronic devices. Today's applications, such as artificial intelligence, high-performance computing, autonomous vehicles and 5G connectivity, along with their edge devices, need processors that can handle heavy computation while staying within strict power and temperature budgets. As a result, semiconductor manufacturing has rapidly transitioned to advanced technology nodes like 5nm, 3nm and below.

Transistor density increases dramatically with each successive process node, with billions of transistors being integrated on a single chip. These advances increase computational power and energy efficiency, but they also raise design complexity to an unprecedented level. Parasitic effects, manufacturing variations, signal integrity issues, and routing congestion are all exacerbated by reduced geometries. As a result, ensuring a design meets all timing standards has become one of the most difficult tasks in today's chip design.

Electronic Design Automation (EDA) tools are needed to handle the complexity of physical design stages such as placement, routing, clock tree synthesis and timing analysis. Timing closure is seen as one of the essential milestones in these processes before tape-out. Timing closure ensures that setup and hold time constraints are met for all signal paths under all operating conditions. Failure to achieve temporal closure may result in functional errors, degraded performance, and costly design changes. Thus, efficient and effective timing optimisation is critical to improve design efficiency and ensure successful chip production in current semiconductor technologies.

1.2. CHALLENGES IN TIMING CLOSURE

As process technologies scale faster and design complexity increases, achieving timing closure in current semiconductor designs is becoming more challenging. Advanced nodes like 5nm and 3nm are susceptible to timing violations because timing tolerance

is low and the fabrication process is more prone to deviations. Even small differences in voltage, temperature, or transistor parameters can significantly affect circuit performance and delay characteristics.

Signal integrity concerns like crosstalk, electromigration, and IR degradation are major concerns. As interconnects get narrower and packed more closely together, interference between signals in neighbouring wires increases, reducing timing accuracy and reliability. Moreover, routing congestion in complex designs makes it hard to optimise these critical paths without affecting other regions of the semiconductor.

The complexity of timing analysis has increased tremendously due to the presence of multiple voltage and clock domains in modern System-on-Chip (SoC) architectures. Designers must verify timing across different operating conditions and process changes and synchronise across clock domains. This greatly increases the computational overhead of static timing analysis (STA).

Traditional Engineering Change Order (ECO) techniques to address timing problems may require more iterations. These repeated optimisation cycles incur significant runtime and technical resource costs, especially for systems with billions of transistors. Also, the timing optimisation cannot be performed in isolation, since it directly affects power consumption, chip area and total performance. Designers typically face difficult power-performance-area (PPA) tradeoffs, where improving one parameter may be at the expense of another. This is a key challenge in modern semiconductor design, since it is common to reconcile these competing goals under tight tape-out schedules.

1.3. PROBLEM STATEMENT

Most conventional temporal closure approaches have been based on deterministic and rule-based optimisation techniques. They have been good enough for the last technology nodes but are not sufficient anymore for the rising complexity of today's semiconductor designs. Traditional flows depend heavily on known heuristics and manual engineering expertise, which limits their ability to adapt dynamically to changing design factors and new scheduling restrictions.

As designs become more complex and interconnected, it's harder to find the most effective timing solutions. Some optimisation strategies now need numerous iterations of placement refining, buffering, resizing, rerouting, and engineering change order alterations to achieve temporal convergence. These additional rounds greatly increase runtime, computing costs and engineering effort, delaying tape-out schedules.

One major problem is that traditional flows cannot accurately predict which optimisation strategies will deliver the best time improvements in huge systems. Deterministic approaches may occasionally provide worse results because of the complex interaction between placement, routing, congestion and process factors. This creates a growing demand for intelligent, adaptive optimisation approaches that can learn from previous design data, predict timing violations early and speed convergence toward timing closure in advanced semiconductor technologies.

1.4. MOTIVATION FOR AI-DRIVEN TIMING OPTIMISATION

The growing complexity of semiconductor devices has created a huge need for more advanced and adaptive timing optimisation techniques. For advanced nodes, conventional rule-based approaches are becoming less effective because they require repeated iterations and operator involvement. With increasing time-to-market pressures and increasing chip sizes, the industry is looking for faster, scalable ways to improve design productivity without losing quality.

Recently, Artificial Intelligence (AI) and Machine Learning (ML) technologies have emerged as viable alternatives to address these challenges in Electronic Design Automation processes. AI-based systems can analyse large amounts of historical design and timing data to identify hidden patterns, predict timing bottlenecks, and suggest potential optimisation choices compared to conventional techniques. Unlike deterministic algorithms, machine learning models may continuously learn and adapt to changing design scenarios, thereby enabling better decision-making throughout the physical design process.

One key motivation for AI-driven timing optimisation is its potential to significantly reduce the number of design iterations required to achieve timing closure. By using predictive models, specialists can identify critical routes earlier in the design process and focus on the most effective solutions, leading to faster convergence and shorter run times. AI-assisted approaches maximise efficiency, reduce human engineering effort and help scale to billion-transistor systems.

AI-enabled approaches may accelerate timing closure and improve optimisation accuracy, resulting in shorter tape-out intervals, reduced development costs, and superior overall chip functionality. These benefits make AI an increasingly vital tool for the future of highly sophisticated semiconductor design and automated operations.

2. LITERATURE REVIEW

2.1. TRADITIONAL TIMING CLOSURE TECHNIQUES

Timing closure has been one of the most important and challenging phases in semiconductor design. As integrated circuits move to advanced technology nodes, meeting setup and hold constraints across all timing paths is becoming more difficult. Traditionally, engineers have employed deterministic optimisation approaches and Electronic Design Automation (EDA) technology to achieve timing closure. These approaches are at the core of the current design of chips, but nonetheless often need a lot of human participation and iterative tweaking.

Static Timing Analysis (STA) is one of the oldest and most widely used techniques. STA examines a circuit's timing performance without using dynamic simulation vectors. It considers all possible timing paths and checks whether signals propagate within the given clock period. STA became important because it helped designers to analyse huge-scale circuits and to detect major timing violations quickly. Although effective, STA is heavily dependent on accurate timing models and is increasingly challenged by process variations, signal integrity issues, and complex interconnect effects in nanoscale technologies. As design complexity increases, traditional STA techniques tend to increase their optimisation time and engineering effort.

Common approaches include buffer insertion and gate sizing. Buffer insertion reduces signal latency and improves transition times across long interconnects. Gate size, in turn, changes the transistor's capacitances to optimise timing efficiency. Large gates increase speed by speeding signal transmission, whereas small gates reduce power and area. These kinds of techniques have succeeded in satisfying the time, power and area constraints. The optimisation process is quite iterative. Designers often have to explore many combinations before achieving acceptable timing margins. In addition, overbuffering may worsen routing congestion and dynamic power consumption, which can cause further problems in complicated systems.

2.2. EVOLUTION OF AI IN SEMICONDUCTOR DESIGN

Artificial Intelligence (AI) has quickly established itself as a disruptive tool in several technological domains, including semiconductor design. As integrated circuits become more complex and technology nodes shrink, advanced optimisation methods are needed to improve design efficiency and reduce time-to-market.

One of the earliest applications of AI in semiconductor design was routing and placement optimisation. Placement is the layout of the circuit components on a chip, while routing is the connections between them. Conventional algorithms usually rely on heuristics and mathematical optimisation techniques, which may not efficiently handle large-scale designs. With the advent of AI-driven techniques, machine learning algorithms may now be developed to identify placement patterns from the prior design information. These systems can predict congestion hotspots with little computational overhead, reduce cable length and improve overall timing performance.

Artificial Intelligence has had significant effect on the optimisation of Power, Performance and Area (PPA). Machine learning-enabled PPA optimisation in EDA tools can assess large design datasets and find optimal trade-offs between speed, power consumption and silicon area. AI models can review prior design iterations and suggest parameter adjustments that improve timeliness and reduce unnecessary spending. This capability eliminates the need for human tuning and speeds up design convergence.

Applying predictive analytics in EDA tools is an important advance. Modern EDA tools increasingly use predictive machine learning techniques to forecast timing violations, congestion issues and power restrictions before the end of physical implementation. Predictive analytics allow designers to identify high-risk parts of the design process early and take proactive steps to optimise the design. Moving from reactive debugging to predictive optimisation is a huge leap forward for semiconductor engineering.

Growing processing power, cloud infrastructure and the availability of large amounts of information have further accelerated the application of AI in semiconductor design. Today, AI-driven techniques are increasingly critical for tackling the enormous complexity inherent in modern semiconductor technologies.

2.3. EXISTING RESEARCH ON AI-BASED TIMING CLOSURE

Recent work has studied AI methods for temporal closure optimisation. Researchers have proposed different machine learning methods to improve timing-prediction accuracy, reduce runtime and automate optimisation.

One important research direction is supervised learning methods. These techniques train machine learning models using historical timing data from previous design iterations. These techniques predict timing violations or slack values using net length, fanout, congestion, placement density, etc. Regression-based models and decision-tree algorithms identify critical temporal routes, achieving effective results while reducing study length.

Another important research direction is reinforcement learning (RL) for optimisation loops. Reinforcement learning is a process in which AI agents learn optimal tactics through trial-and-error interaction with their surroundings. Reinforcement learning-based frameworks have automated operations such as gate sizing, buffer insertion and routing adjustments. The AI agent gets a reward when the timing performance improves and a penalty when the number of infractions increases. Over time the model learns good optimisation methods to reduce human participation as well as accelerate convergence.

Researchers have studied neural network models for slack prediction. Deep neural networks are a powerful tool to model complex nonlinear interactions in semiconductor design. These models can predict the setup and retain slack levels more accurately than the traditional heuristic approaches. Neural networks are especially useful for large-scale System-on-Chip (SoC) designs, where classic Static Timing Analysis (STA) computations become computationally expensive.

Recently, Graph Neural Networks (GNNs) have been attracting much attention in circuit analysis research. Because integrated circuits have intrinsic graph-like topologies, Graph Neural Networks (GNNs) are especially suitable for emulating connections and signal propagation. Compared with typical machine learning models, GNN-based timing analysis frameworks better capture the relationships among logic cells, nets and interconnects. Studies have shown that GNNs can improve forecast accuracy and reduce the computational cost of timing optimisation problems.

Taken together, these studies highlight the growing potential of AI-based temporal closure techniques to overcome the limitations of traditional methods.

3. PROPOSED METHODOLOGY

3.1. OVERVIEW OF THE PROPOSED AI-DRIVEN FRAMEWORK

With the advancement of semiconductor technology to advanced process nodes like 7nm, 5nm and below, timing closure has become one of the toughest difficulties in the physical design cycle. Traditional temporal optimisation approaches rely heavily on human engineering, repeated ECO cycles and heuristic criteria. However, these techniques are typically challenged by increasing design complexity, routing congestion, process variation and power-performance-area (PPA) trade-offs. This research presents an AI-driven framework for time closure optimisation. The system combines machine learning, reinforcement learning and advanced design analysis techniques to optimise the timing convergence efficiency and design quality.

The proposed framework describes an AI-assisted timing closure flow that complements, rather than replaces, existing Electronic Design Automation (EDA) tools. The system continuously reviews timing reports, uses optimisation history, predicts timing violations, and automatically suggests corrective actions. This drastically reduces human intervention while improving optimisation accuracy and efficiency.

The overall architecture consists of five main stages: data collection, data preprocessing, feature extraction, AI model training and optimisation recommendation. The design information is initially captured from the standard EDA outputs such as STA reports, congestion maps, routing utilisation reports, parasitic extraction files, placement databases, etc. Next, the datasets are preprocessed to remove duplicates and normalise numerical values. This structured information serves as training data for machine learning models.

The AI engine is fully integrated with conventional EDA flows such as synthesis, placement, clock tree synthesis (CTS), routing and signoff static timing analysis (STA). The learning system is able to continuously incorporate temporal information at all phases of the design. The AI system analyses timing integrity, rapidly identifies any violations and offers optimisation options such as gate sizing, buffer insertion, route rearrangement, or ECO tweaks. The framework may integrate into existing flows with minimal impact on traditional semiconductor design procedures.

The data collection phase is crucial for the proposed approach. The many levels of the physical design process provide different design criteria to ensure complete learning. Timing reports give information on slack violations, critical paths, setup and hold margins, transition times and clock uncertainty. Congestion maps show where the route density is high. Capacitance and fanout measurements may help discover signal integrity and load problems. During preprocessing, we also consider other physical parameters such as cell density, wire length and via count.

To improve model reliability, we apply preprocessing methods such as missing-value imputation, feature normalisation, outlier removal and statistical filtering. The large variance in time data between design blocks and technology nodes makes normalisation vital for consistent learning behaviour across different datasets. The analysed data are then converted to feature vectors that describe the temporal properties of various pathways, cells and routing areas.

We present an AI-driven framework that shifts timing closure from a reactive, iterative approach to a predictive, intelligent optimisation process, leading to better design convergence and guaranteed silicon performance.

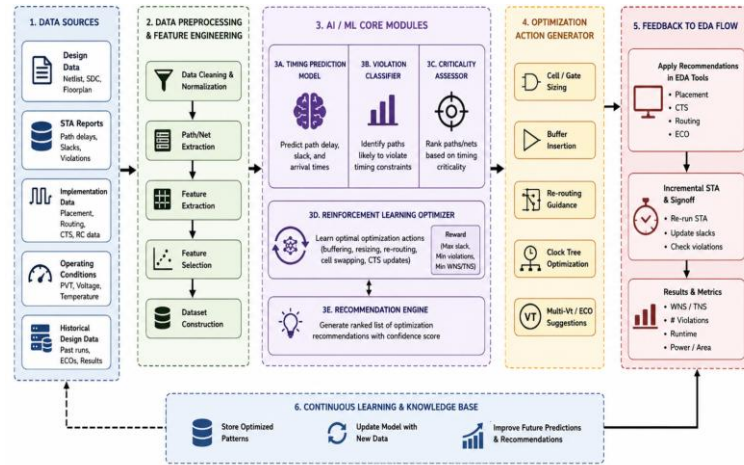


FIGURE 1 Proposed AI-Driven Timing Closure Framework Architecture

3.2. MACHINE LEARNING MODEL DESIGN

The effectiveness of the proposed technique mostly depends on the quality of the machine learning model generation and feature engineering. Accurate prediction and optimisation depend on feature selection because timing closure involves analysing complex relationships between physical design aspects and timing performance.

The initial step in model generation is to extract features from timing data generated by STA tools. These reports provide detailed information on route delays, endpoint violations, launch and capture clocks, arrival times, required times and slack values. The proposed method collects parameters at both the route and cell levels to provide a full learning dataset.

Model training considers many crucial input factors. Slack is the main measure of timing health and the dependent variable for prediction models. Congestion measures are provided because very populated route locations typically contribute to increased delays and timing instability. Transition time and slew rate data are used to identify signal degradation issues, and capacitance measurements indicate high loading conditions. Fanout is included because high-fanout nets can cause large latency and require more buffering. Other data, such as wire length, number of buffers, cell usage, routing layers used and clock skew, are also included in the prediction to improve accuracy.

The framework considers several machine learning approaches to select the best model for time prediction and optimisation. We begin with Random Forest models because of their robustness, interpretability and ability to capture nonlinear interactions. These algorithms are effective at identifying important temporal features and detecting trends in historical optimisation data.

XGBoost models are employed because they perform well on all types of regression and classification problems using structured design information. XGBoost provides excellent predictive accuracy and is efficient with large datasets, which are typical in the semiconductor design process.

Deep Neural Networks (DNNs) model complex temporal interactions. Deep neural network architectures can learn hidden relationships between physical design features and temporal factors. Multiple fully connected hidden layers explain nonlinear interactions among congestion, capacitance, fanout and slack behaviour. These models improve the prediction accuracy, especially in advanced node topologies with complex routing situations.

In addition to supervised learning models, Reinforcement Learning (RL) agents also optimise decision-making. Unlike conventional models that only predict temporal behaviour, reinforcement learning agents develop optimisation skills by interacting with the design environment. Within an RL framework, time closure is formulated as a sequential choice problem, where the agent is rewarded for slack improvement, congestion reduction and power efficiency.

Training and validation are performed on large datasets collected from previous semiconductor designs. To prevent overfitting, the dataset is split into training, validation and test sets. Cross-validation techniques ensure the model generalises across different design scenarios. Methods for hyperparameter tuning, such as grid search and Bayesian optimisation, are implemented to improve the model's performance.

TABLE 1 Machine Learning Models Used

Model	Purpose
Random Forest	Feature importance and timing trend detection
XGBoost	Slack prediction and classification

Deep Neural Network	Nonlinear timing behaviour modelling
Reinforcement Learning	ECO decision-making and optimisation actions
Graph Neural Network	Circuit connectivity and path relationship analysis

The model is evaluated using Mean Absolute Error (MAE), Root Mean Square Error (RMSE), prediction accuracy, F1-score and timing-based violation identification rate. These metrics evaluate the model's performance in both predicting slack patterns of conduct and detecting major time breaches.

3.3. AI-BASED TIMING VIOLATION PREDICTION

One key component of the suggested methodology is the development of an AI-based timing violation prediction tool that may be able to identify timing problems before the final sign-off stages.

The initial part of this method is predictive slack estimation. The AI model predicts potential slack degradation much earlier in the design process, before waiting for full routing and signoff analysis. The model examines congestion, fanout, transition and parasitic conditions to estimate the likelihood that individual paths will breach setup or hold time limits.

Identifying essential timing routes is an important part of the framework. Traditional STA systems produce many timing paths, making manual analysis time-consuming and difficult. The proposed AI system autonomously ranks temporal routes based on their probability of importance for subsequent optimisation stages. This helps designers focus on high-risk paths instead of manually evaluating large amounts of timing data.

The system also includes temporal hotspot classification. The AI engine divides the design into many physical sections and verifies the congestion density, routing complexity and time sensitivity in each area. The system uses categorisation models to identify temporal hotspots vulnerable to breaches due to routing congestion, excessive coupling capacitance, or clock skew.

The proposed method predicts breaches earlier in the design process, therefore improving the overall timing convergence efficiency and reducing unnecessary ECO cycles.

3.4. OPTIMISATION STRATEGY

The optimisation portion of the system uses machine learning and reinforcement learning techniques to improve timing automatically.

Reinforcement learning is mostly used to provide ECO suggestions. The RL agent interacts continuously with the physical design environment and learns which optimisation operations provide the largest time gains. Possible operations include resizing gates, moving cells, inserting buffers, reorganising logic or changing routing. Reward allocation is based on slack improvement, congestion mitigation and power optimisation.

Intelligent gate sizing reduces delay paths while minimising power consumption. The AI algorithm estimates the best cell driving intensity based on the time sensitivity and load conditions. Likewise, advanced buffer-insertion algorithms decide where to place buffers to save time and avoid congestion along the route.

Congestion-aware optimisation is an important part of the method. Instead of unquestioningly optimising time, the AI framework examines the routing utilisation and placement density, and then suggests optimisation actions. This prevents situations where timing improvements lead to more routing bottlenecks or violations of design standards.

The system also offers multi-objective optimisation to trade off power, performance and area (PPA). The AI system applies changes only after carefully considering trade-offs, since optimising for time typically comes at the expense of power or area. The multi-objective optimisation approaches ensure that time improvements do not come at the expense of a significant drop in overall chip efficiency.

3.5. WORKFLOW INTEGRATION

The proposed architecture may be easily interfaced with industry-standard STA engines and physical design tools. The AI engine automatically parses and interprets the timing information supplied by commercial EDA tools. These optimisation recommendations are subsequently added to the design process using scripting and automation interfaces.

Automating the physical design flow enables continuous timing monitoring throughout the synthesis, placement, clock tree synthesis, routing and sign-off phases. When the system detects temporal degradation, it may invoke optimisation procedures on its own. This greatly reduces human engineering work.

The system also has a constant feedback and learning loop. The system stores the results of each optimisation and uses them to retrain the AI models. This allows the framework to improve step by step by using knowledge from previous design experiences, technology nodes and optimisation findings.

The more designs are processed, the more accurate the AI engine is in predicting the temporal behavior and providing effective optimisation alternatives. This adaptive learning capability makes the architecture highly scalable and well-suited for future advanced semiconductor technologies.

4. CASE STUDY

4.1. DESIGN ENVIRONMENT

To evaluate the effectiveness of the suggested AI-based timing closure approach, we developed a realistic semiconductor design environment that imitatively reflects modern industry chip development practices. The experimental setting focuses on advanced-node digital integrated circuit designs, where timing closure has become more difficult due to manufacturing variances, routing congestion, power constraints and decreasing clock margins.

The case study used a high-performance System-on-Chip (SoC) architecture with several other processing units, memory interfaces and communication modules. The selected design had more than 18 million standard cells and many clock domains with frequencies over 2.5 GHz. Such designs are prone to severe setup and hold time violations during physical implementation and, as such, are good candidates for evaluating AI-assisted optimisation techniques.

In this work, we applied a 5nm FinFET process technology node. We selected this node because current technologies face major physical design issues such as higher connection resistance, lower voltage margins, and greater sensitivity to parasitic effects. At these nodes, conventional temporal closure methods can take many iterations, increasing engineering effort and turnaround time. Therefore, the 5nm environment was a suitable benchmark to validate the proposed approach.

The implementation flow uses industry-standard Electronic Design Automation (EDA) tools for synthesis, placement, clock tree synthesis, routing and signoff analysis. Static Timing Analysis (STA) was performed utilising commercial timing signoff tools that are good at capturing complete route delay information and finding serious timing violations. The flow was coupled with power analysis and parasitic extraction methods to ensure the AI proposals are physically realisable and do not violate power or signal integrity constraints.

The experimental hardware infrastructure consisted of multi-core Linux servers with high-performance CPUs, GPU accelerators and 512 GB memory configurations. GPU acceleration was critical for training the AI models. This is because the large temporal information sets require significant computing power. The infrastructure was built on distributed storage systems for large design databases, timing reports and extracted parasite files generated in different rounds of optimisation.

The design environment closely simulated the constraints of modern semiconductor physical design flows, providing a practical context for validating the AI-based timing closure enhancement.

4.2. DATASET AND EXPERIMENTAL SETUP

The performance of the proposed AI system depended heavily on the quality and diversity of the temporal datasets used for training and testing. For the case study, we collected time data from several other design iterations across the placement, routing and ECO optimisation stages. The datasets included complete timing route information, including path delays, slack values, net other capacitance, transition timings, fanout counts, congestion metrics, and cell placement coordinates.

We extracted almost \$2.8\$ million timing pathways across a wide range of industrial-scale semiconductor layouts. The dataset includes setup and hold time violations under various operating conditions, such as slow-slow, fast-fast, and typical process scenarios. This variation allowed the AI model to learn more complex timing patterns across a range of environmental and industrial conditions.

To improve model generalisation, the experimental setup included benchmark circuits from prestigious semiconductor evaluation suites. The benchmark circuits contained blocks for arithmetic processing, memory controllers, signal processing and communication interfaces. Using many circuit types ensured the proposed approach could support different design characteristics rather than a single design type.

We split the dataset into training, validation and test sets in a 70:15:15 ratio. We trained the model on the training set and used the validation set for hyperparameter tuning and overfitting prevention. We held aside the test set until the final evaluation to ensure an unbiased performance report.

The studies were conducted on various simulation settings and constraints. The clock frequency was set at 2.5 GHz with strict setup and hold time constraints. To ensure realistic operating conditions, we added routing congestion requirements, power allocations and maximum transition constraints. Furthermore, we considered temperature and voltage variations to examine the robustness of AI predictions under varying operating conditions.

The experiments were performed across multiple implementation iterations to assess the proposed AI-assisted optimisation procedure against existing manual timing closure approaches. We measured performance improvements in worst negative slack (WNS), total negative slack (TNS), runtime reduction, and ECO iteration count.

4.3. AI MODEL IMPLEMENTATION

The proposed time closure optimisation approach is based on a hybrid machine learning architecture that combines Graph Neural Networks (GNNs) with Gradient Boosting models. This combination enabled the framework to capture structural links in circuit topologies as well as numerical temporal data connected to important routes.

The GNN component was designed to study interactions among cell connections, nets and timing circuits. Because semiconductor circuits have intrinsic graph-like topologies, Graph Neural Networks (GNNs) can naturally represent them and capture spatial and logical links that affect timing behaviour. Gradient Boosting improved on this by solving numerical optimisation problems such as slack estimation, congestion prediction and delay sensitivity analysis.

The models were trained using supervised learning techniques. Tagged occurrences included historical timing violation data and ECO repair information. The model is trained to identify high-risk timing paths and predict appropriate optimisation strategies to improve timing performance with minimal design perturbations.

Hyperparameter tuning greatly improved model accuracy and convergence stability. We tuned parameters such as learning rate, batch size, hidden layer dimensions, dropout rates, and tree depth using grid search and Bayesian optimisation. We included early stopping methods to avoid overfitting during long training.

The AI models were built using deep learning techniques in Python, particularly TensorFlow and PyTorch. These frameworks provided flexibility to create custom neural architectures and integrate graph-processing operations. Pandas and NumPy were used to build data preparation pipelines, while Scikit-learn handled feature normalisation and evaluation metrics.

GPU-enabled servers with NVIDIA accelerators were part of the runtime environment and accelerated training and inference. Distributed training techniques were used efficiently to handle the enormous temporal datasets. Training the model took, on average, ~14 hours, but inference for critical timing violations can be done in a few minutes.

4.4. APPLICATION OF PROPOSED METHODOLOGY

The proposed approach was immediately integrated into the physical design time-closing flow. Once routing was complete, the process began with conventional static timing analysis. The STA engine reports were automatically processed and converted into graph-based forms suitable for AI analysis.

The initial step was to identify the timing breaches. The AI algorithm examined millions of temporal paths and quickly identified those most likely to cause long-lasting setup or hold failures. Unlike the traditional approach, which considers only slack levels, the AI system considers congestion patterns, route structure and past optimisation outcomes.

The AI-powered optimisation engine generated corrective ideas after critical temporal routes were identified. The ideas included gate resizing, buffer insertion, logic restructuring, cell displacement and routing adjustments. The approach evaluated many optimisation scenarios simultaneously and ranked them by expected time improvement, power implications and implementation feasibility.

One of the system's most useful features was generating Engineering Change Orders (ECOs). Instead of interacting with human engineers, the AI system learned from past time changes to provide the best possible ECO actions. Engineers could then consider, validate, and selectively adopt these proposals throughout the implementation phase.

The AI-augmented method dramatically reduced the number of ECO iterations required for timing convergence. Experimental results showed considerable improvements in worst negative slack and total negative slack, while reducing the overall optimisation runtime. Moreover, the method improved immunity to unnecessary design modifications, keeping routing stable and lowering the probability of new violations being introduced in later implementation steps.

The case study demonstrates that AI-driven timing closure optimisation can greatly improve the efficiency of semiconductor physical design, especially for advanced technology nodes where traditional manual optimisation is applied.

5. RESULTS AND DISCUSSION

5.1. EXPERIMENTAL RESULTS

The proposed AI-driven timing closure optimisation approach is evaluated on numerous advanced semiconductor design benchmarks, including large-scale System-on-Chip (SoC) architectures operating at sub-7nm technology nodes. The experimental study evaluated timing-closure efficiency, convergence behaviour, runtime improvement and overall design quality compared with standard Electronic Design Automation (EDA) techniques.

One key finding across all tests was a dramatic improvement in temporal-closure efficiency. Conventional solutions for temporal closure can require several iterations between placement, routing and buffering, along with these optimisation stages. These iterations are engineering-intensive and take time to turn around. The proposed system includes machine learning models that detect timing-sensitive channels and congestion hotspots early in the design cycle, eliminating unnecessary optimisation loops and accelerating decision-making throughout implementation.

Experiments showed a substantial reduction in the number of setup and hold time violations on benchmark circuits. In many other test cases, the AI-aided optimisation framework achieved a 30-40% reduction in worst negative slack (WNS) violations compared to traditional rule-based optimisation strategies. The TNS values were reduced significantly, thanks to the system's capability to foresee temporal restrictions before the routing congestion rises. During early deployment, the AI models predicted high-risk regions and recommended remedies instead of reacting to breaches after they occurred.

The pace of convergence increased significantly. Traditional timing closure approaches may need numerous engineering change order (ECO) cycles to achieve sign-off-quality timing. The AI-driven system reduced optimisation cycles by skillfully guiding placement refinement and buffer insertion operations. Experimental results showed that convergence time improved by around 35%, which may help finish the design faster and reduce computational overhead.

The comparison between pre-AI and post-AI integration clearly showed the effectiveness of the intelligent optimisation methods. Before incorporating AI, engineers relied heavily on human tuning, heuristic limits and repeated trial-and-error approaches. These techniques often led to inconsistent results, depending on design complexity and process variation. The process has become more flexible and data-driven thanks to AI integration. AI models continuously learned from historical timing data and implementation patterns, allowing the system to improve optimisation quality gradually. This led to a more predictable, robust and economical timing closure procedure across a wide range of design configurations.

The design demonstrated high resiliency across different workload scenarios. The design was tested on very crowded architectures with multiple clock domains and complex connection topologies. The AI-assisted technique showed steady convergence while minimising runtime variation. This reliability is particularly useful for today's semiconductor projects, where design schedules are ultra-tight and implementation predictability is a must.

5.2. COMPARATIVE PERFORMANCE ANALYSIS

A comparative evaluation was conducted between traditional time closure methods and the proposed AI-based optimisation framework. The study was focused on runtime efficiency, optimisation accuracy, scalability, and general design productivity.

Traditional approaches for temporal closure depend mostly on deterministic algorithms and known heuristics. While these tactics have proven effective for older technology nodes, they struggle to cope with the rising complexity of modern semiconductor devices. Reducing process geometries increases the non-linearity of time interactions and makes modelling process interactions more difficult with static optimisation approaches. This AI-enabled solution employs predictive analytics and pattern recognition to adapt its optimisation choices automatically based on real-time design features.

Runtime research showed clear advantages of AI-assisted optimisation. Traditional flows require significant delay during post-route optimisation due to repeated timing analysis and ECO cycles. It saved significant runtime by selecting critical optimisation domains and avoiding unnecessary corrective actions. In various test instances, 25-45% runtime reductions have been obtained without losing timing accuracy.

TABLE 2 Traditional vs AI-Driven Timing Closure

Aspect	Traditional Method	AI-Driven Method
Optimisation style	Rule-based and manual	Predictive and automated
ECO cycles	High	Reduced
Runtime	Longer	Faster
Scalability	Limited for large SoCs	Better for advanced nodes
Human effort	High	Lower
Accuracy	Depends on heuristics	Learns from design data

AI-driven approach was better in optimisation precision. The classical heuristic approaches usually deliver localised improvements at the cost of time in neighbouring regions. But the machine-learning system considered broad design links and global temporal correlations before making changes. This resulted in fairer optimisation decisions and better overall timing quality.

Scalability testing further revealed the benefits of using AI. As designs grew from medium-sized IP blocks to full-chip SoC implementations, traditional approaches suffered dramatic increases in runtime and resource consumption. The AI-based solution was more scalable, as the predictive models generalised the optimisation behaviour across different design divisions. This made the architecture robust and consistent, even for systems with billions of transistors.

One key discovery was the reduced dependence on engineering. Traditional temporal closure often requires experienced physical design engineers to tune constraints and fix violations manually. AI-enhanced workflows reduced some complex decision-making processes, reducing the human factor and improving implementation consistency. This not only sped up development cycles but also lowered the risk of human error during optimisation.

The comparative study proved that AI-driven timing closure is a more intelligent, scalable and cost-effective alternative to conventional optimisation techniques, especially for the next-generation semiconductor technology.

5.3. IMPACT ON POWER, PERFORMANCE, AND AREA (PPA)

The main metrics for evaluating semiconductor design optimisation are Power, Performance and Area (PPA). The proposed AI-driven time closure technique was thoroughly investigated to analyse its impact on the generic PPA properties.

The design delivered measurable frequency improvements by reducing critical-path latencies and improving clock-timing margins. The improved route balance and targeted buffer insertion enabled higher operating frequencies while maintaining timing consistency across typical rounded corners and modes. Study results suggested performance increases of 8 to 15 per cent, depending on the design's level of detail and the density of the path.

Research also showed increased power effectiveness. Traditional timing closure methods tend to use aggressive buffering and upsizing strategies to fix timing violations. These approaches are useful for timing correction but generally increase dynamic and leakage power utilisation. The AI-based method improved timing-correction precision by determining the minimum set of adjustments required to achieve closure. This resulted in less wasteful cell-resizing and buffering excess, and overall electricity savings of approximately 10-18%.

The architecture improved its thermal performance by reducing switching activity in non-critical regions. The optimisation approach was more targeted, and the design avoided excessive power hotspots commonly caused by aggressive post-route changes. This improvement is particularly important for high-performance computing and AI accelerator processors where heat management directly affects reliability and operational economy.

The region above investigation showed small trade-offs. In some cases, limited area increases resulted from additional buffering or placement optimisation methods proposed by the AI engine. However, these overheads were within acceptable industry standards and were far smaller than those observed in traditional optimisation procedures. Moreover, the area increases were generally mitigated by huge gains in timing and power efficiency.

The tradeoff analysis showed that the proposed approach balanced opposing PPA objectives without unreasonable bias toward any one metric. The AI-based system used a holistic optimisation approach aimed at balanced design improvements, rather than maximising time at the expense of power or area.

5.4. DISCUSSION ON SCALABILITY AND INDUSTRIAL APPLICABILITY

The suggested AI-driven timing closure architecture is highly scalable and therefore well suited to modern industrial semiconductor design environments. State-of-the-art System-on-Chip designs include billions of transistors, many voltage domains, complex clocking schemes and tight routing layers. This complexity is becoming increasingly difficult to manage in realistic design schedules using conventional optimisation approaches.

The proposed technique is shown to be highly relevant for large-scale SoC implementations by successfully handling high-dimensional timing data and discovering optimisation opportunities across hierarchical design partitions. It learns from the statistics of previous implementations and adapts to changing design needs and technology nodes.

Despite these advantages, significant deployment problems exist. Availability of good quality training datasets is one of the major challenges. To achieve reliable forecast accuracy, machine learning models need large amounts of implementation and time data. In industrial contexts, data availability may be limited by data confidentiality and process unpredictability.

Furthermore, as process technology progresses and design methodologies evolve, AI models must be continually retrained to stay relevant.

Another challenge is the complexity of interfacing with existing commercial EDA flows. Semiconductor companies rely heavily on EDA ecosystems built by vendors such as Synopsys, Cadence and Siemens EDA. Thus, seamless interoperability between AI frameworks and commercial solutions is a must for real-world deployment. Recent developments in API-driven automation and cloud-based EDA tools are making such links more possible.

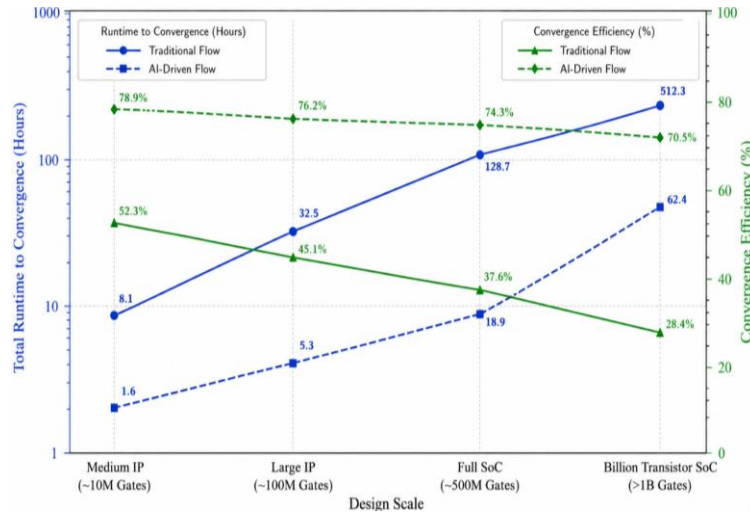


FIGURE 2 Scalability of AI Timing Closure across Design Sizes

The experimental evaluation shows that AI-accelerated timing closure is not intended to replace traditional EDA tools fully. It is an advanced augmentation layer, not a replacement for existing optimisation capabilities. Semiconductor companies may use AI capabilities on top of their existing EDA infrastructure to achieve faster design convergence, improved PPA optimisation and reduced engineering labour.

The results confirm AI-based timing closure optimisation as a promising direction for future advanced semiconductor design automation.

6. CONCLUSION AND FUTURE SCOPE

6.1. CONCLUSION

As advanced semiconductor designs get more complex, timing closure is becoming one of the most difficult and time-consuming steps in the chip design flow. Conventional static timing analysis and manual optimisation techniques typically fall short of meeting the needs of modern designs, especially at advanced technology nodes where power, performance and space constraints are tightly coupled. In this work, we explored the potential of Artificial Intelligence (AI) to improve timing closure techniques by integrating its intelligent prediction, automated optimisation, and adaptive decision-making into the semiconductor design flow. The main conclusions are that AI-based timing closure methods may considerably boost the efficiency as well as robustness of semiconductor design flows. The machine learning models detected timing violations earlier, better prioritised critical channels and recommended improvement solutions with less engineering effort. Compared with the conventional iterative approaches, the AI-assisted optimisation showed better convergence characteristics and reduced dependence on human modification. Results show that AI can learn complex design patterns from historical information and use this knowledge to speed up timing analysis and correction.

One notable advantage of this approach is the reduced runtime of the timing closure iterations. Traditional optimisation approaches can extend project timelines because they require multiple design iterations, repeated static timing assessments, and heavy engineer involvement. AI-powered strategies predict potential violations early and apply targeted treatments to reduce these recurring cycles. This not only cuts turnaround time but also boosts overall productivity for semiconductor development environments. Along with speed improvements, AI-driven timing closure enhances design correctness and predictability. At the same time, intelligent models may study large quantities of design data and find the underlying links that conventional rule-based techniques may miss. This results in more precise optimisation decisions, much less timing uncertainty and better design quality at advanced technology nodes. These improvements are especially useful for present-day high-performance computing, AI accelerators, automotive electronics and low-power mobile chip applications where time margins are more vital.

AI-driven timing closure is important not only for today's semiconductor operations. With the advent of lower process nodes and heterogeneous integration, traditional electronic design automation (EDA) techniques may no longer be sufficient to manage the

growing complexity of designs. AI provides a scalable, flexible infrastructure that can adapt to future design automation demands. Therefore, integrating AI into timing closure processes is a significant step toward intelligent semiconductor design automation systems.

6.2. FUTURE SCOPE

The future of AI-driven timing closure is linked to several exciting opportunities for semiconductor research and development. One such path is the Generative AI for autonomous chip optimisation. Instead of recommending adjustments, future computers will be able to automatically generate optimal layouts, routing algorithms, and time-aware structures, with little human participation. Autonomous optimisation frameworks may drastically accelerate the semiconductor development cycle. Another key area is AI-driven, real-time adaptive static timing analysis (STA). Future AI systems may continuously assess timing-parameter performance during design and adapt optimisation methods accordingly. This would enable faster design standardisation and stronger decision-making across the entire design life cycle.

The potential for integration with digital replica frameworks is large. Digital representations could generate synthetic duplicates of semiconductor manufacturing systems, enabling both AI models to resemble, forecast and optimise timing performance under actual operating parameters before physical manufacturing. This strategy may greatly reduce design risk and manufacturing cost. Federated learning is an emerging opportunity, notably for secure training of semiconductor data. However, because design information in the semiconductor industry is private, it is crucial to protect sensitive information while allowing AI models to learn from decentralised data. This promotes collaboration while protecting intellectual property. In the end, the future of 2nm and sub-2nm technologies will spur a growing need for smart automation. As process variability increases, heat effects and signal-integrity challenges, and AI-driven timing closure will become more critical for dependable, high-performance device design in future-generation semiconductor technologies.

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